What is claimed is:

1. A method for performing DMA transfers with dynamic descriptor structure, comprising the steps of:

creating a new chain of descriptors each including an end-of-chain entry set to a false value except a dummy descriptor at the end of the new chain having the end-of-chain entry set to a true value, wherein each of the descriptors excluding the dummy descriptor further comprises one or more parameters identifying data to be transferred and a link pointer specifying a next descriptor within the new chain;

appending the new descriptor chain to a previous descriptor chain, if any, by transferring the parameters and the link pointer of the first descriptor within the new descriptor chain to a dummy descriptor of the previous descriptor chain;

changing the end-of-chain entry of the dummy descriptor within the previous descriptor chain from the true value to the false value;

fetching the descriptor specified by a next address;

determining whether the end-of-chain entry of the currently fetched descriptor is set to the false value;

if so, updating the next address with the link pointer of the currently fetched descriptor; and

transferring the data identified in the parameter of the currently fetched descriptor.

2. The method as recited in claim 1 further comprising the step of issuing a command after the new descriptor chain is appended to the previous descriptor chain.

3. The method as recited in claim 2 further comprising the step of causing the next address to point to the first descriptor within the new descriptor chain before the issuing step.

4. The method as recited in claim 2 further comprising the step of ignoring the issued command if the data transfer identified in the previous descriptor chain is being performed.

5. The method as recited in claim 2 further comprising the step of accepting the issued command if there are no more data transfers identified in the previous descriptor chain.

6. The method as recited in claim 1 wherein the fetching step through the transferring step are executed in a loop until the end-of-chain entry with the true value is detected in the determining step.

7. The method as recited in claim 5 wherein, after acceptance of the issued command, the fetching step through the transferring step are executed in a loop until the end-of-chain entry with the true value is detected in the determining step.

8. A method for performing DMA transfers under control of a DMA controller and a processor, the method comprising the steps of:

creating a chain of descriptors each including an end-of-chain entry set to a false value except a dummy descriptor at the end of the descriptor chain having the end-of-chain entry set to a true value, wherein each of the descriptors excluding the dummy descriptor further comprises one or more parameters identifying data to be transferred by the DMA controller and a link pointer specifying a next descriptor within the descriptor chain;

causing a starting address to point to the first descriptor within the descriptor chain;

issuing a start command by the processor;

accepting the start command by the DMA controller which is in an idle state;

replacing a next address with the starting address;

from the descriptor chain, fetching the descriptor specified by the next address;

determining whether the end-of-chain entry of the currently fetched descriptor is set to the false value;

if so, updating the next address with the link pointer of the currently fetched descriptor;

transferring the data identified in the parameters of the currently fetched descriptor; and

repeating the fetching through the transferring steps until the end-of-chain entry with the true value is detected in the determining step.

9. The method as recited in claim 8 further comprising the steps of:

creating a new chain of descriptors;

appending the newly created descriptor chain to the previously created descriptor chain by transferring parameters and a link pointer of the first descriptor within the newly created descriptor chain to the dummy descriptor of the previously created descriptor chain;

changing the end-of-chain entry of the dummy descriptor within the previously created descriptor chain from the true value to the false value;

issuing a resume command by the processor; and

ignoring the resume command if the data transfer identified in the previously created descriptor chain is being performed by the DMA controller.

10. The method as recited in claim 9 further comprising the step of accepting the resume command by the DMA controller if there are no more data transfers identified in the previously created descriptor chain.

11. The method as recited in claim 10 wherein, after acceptance of the resume command, the fetching through the transferring steps are resumed in a loop until the end-of-chain entry with the true value is detected in the determining step.

12. A method for performing DMA transfers under control of a DMA controller and a processor, the method comprising the steps of:

creating a chain of descriptors each including an end-of-chain entry set to a false value except the last descriptor within the descriptor chain having the end-of-chain entry set to a true value, wherein each of the descriptors further comprises one or more parameters identifying data to be transferred by the DMA controller and a link pointer specifying a next descriptor within the descriptor chain;

causing a next address to point to the first descriptor within the descriptor chain;

issuing a command by the processor;

accepting the issued command by the DMA controller which is in an idle state;

from the descriptor chain, reading the descriptor specified by the next address;

transferring the data identified in the parameters of the currently read descriptor;

determining whether the end-of-chain entry of the currently read descriptor is set to the false value;

if so, updating the next address with the link pointer of the currently read descriptor; and

repeating the reading through the updating steps until the end-of-chain entry with the true value is detected in the determining step.

13. The method as recited in claim 12 further comprising the steps of:

creating a new chain of descriptors;

appending the newly created descriptor chain to the previously created descriptor chain by causing the link pointer of the last descriptor within the previously created descriptor chain to point to the first descriptor within the newly created descriptor chain;

changing the end-of-chain entry of the last descriptor within the previously created descriptor chain from the true value to the false value;

issuing the command by the processor; and

ignoring the issued command if the data transfer identified in the previously created descriptor chain is being performed by the DMA controller.

14. The method as recited in claim 13 further comprising the steps of:

if there are no more data transfers identified in the previously created descriptor chain:

accepting the issued command by the DMA controller;

fetching the descriptor specified by the next address; and

replacing the next address with the link pointer of the currently fetched descriptor.

15. The method as recited in claim 14 wherein, once the issued command is accepted by the DMA controller, the

reading step through the updating step are executed in a loop until the end-of-chain entry with the true value is detected in the determining step.